14:47:06 OCA PAD INITIATION - PROJECT HEADER INFORMATION 03/01/95

Active

Project #: E-21-Z23 Cost share #: Rev #: 0
Center # : 10/24-6-R8440-0A0 Center shr #: OCA file #:
Work type : RES
Contract#: N66604-95-M-BZ39 Mod #: Document : PO
Prime #: Contract entity: GTRC

Subprojects ? : N CFDA:
Main project #: PE #:

Project unit: ECE Unit code: 02.010.118
Project director(s):
ALLEN M G ECE (404)894-2902

Sponsor/division names: NAVY / NAVAL UNDERWATER SYS, RI
Sponsor/division codes: 103 / 049

Award period: 950127 to 950615 (performance) 950615 (reports)

Sponsor amount	New this change	Total to date
Contract value	10,000.00	10,000.00
Funded	10,000.00	10,000.00
Cost sharing amount		0.00

Does subcontracting plan apply ?: N

Title: FABRICATION OF MICROMACHINED MAGNETIC MICROTILES

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Security class (U,C,S,TS) : U ONR resident rep. is ACO (Y/N): N
Defense priority rating : N/A GOV supplemental sheet
Equipment title vests with: Sponsor X GIT
NONE PROPOSED
Administrative comments -
INITIATION.

GEORGIA INSTITUTE OF TECHNOLOGY
OFFICE OF CONTRACT ADMINISTRATION

NOTICE OF PROJECT CLOSEOUT

Closeout Notice Date 08/09/95

Project No. E-21-Z23_____ Center No. 10/24-6-R8440-0A0_

Project Director ALLEN M G_____ School/Lab ECE_____

Sponsor NAVY/NAVAL UNDERWATER SYS, RI_____

Contract/Grant No. N66604-95-M-BZ39_____ Contract Entity GTRC

Prime Contract No. _____

Title FABRICATION OF MICROMACHINED MAGNETIC MICROTILES_____

Effective Completion Date 950615 (Performance) 950615 (Reports)

Closeout Actions Required:	Y/N	Date Submitted
Final Invoice or Copy of Final Invoice	Y	_____
Final Report of Inventions and/or Subcontracts	N	_____
Government Property Inventory & Related Certificate	N	_____
Classified Material Certificate	N	_____
Release and Assignment	N	_____
Other _____	N	_____

Comments_____

_____

Subproject Under Main Project No. _____

Continues Project No. _____

Distribution Required:

Project Director	Y
Administrative Network Representative	Y
GTRI Accounting/Grants and Contracts	Y
Procurement/Supply Services	Y
Research Property Managment	Y
Research Security Services	N
Reports Coordinator (OCA)	Y
GTRC	Y
Project File	Y
Other _____	N
_____	N

Fabrication of Micromachined Magnetic Microtiles

David J. Coe , Eric M. Panning, and Mark G. Allen
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Atlanta, Georgia

1.0 Introduction

Fabrication of the Lorentz force actuator may be divided into two steps, flux guide fabrication and electrode fabrication. In our preliminary investigation, we have focused on developing a procedure for fabricating the magnetic flux guide since this seems to be the more difficult problem to solve.

2.0 Flux Guide Test Structure

2.1 Description

Magnetic flux will be guided through the silicon substrate in an electroplated nickel/iron plug which extends from the front surface of the wafer to the back surface. Figure 1 shows a cross section of the test structure.

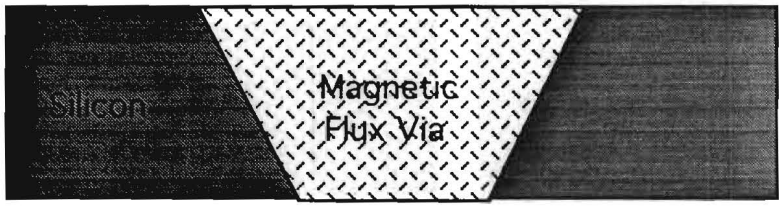

Figure 1 Cross section of flux guide test structure.

The selection of an 80% nickel / 20% iron alloy (permalloy) allows for saturation flux densities on the order of 1.0 Tesla. Saturation densities up to 1.5 Tesla may be achieved using other nickel/iron alloys.

2.2 Fabrication Procedure

Test structure fabrication consists of two parts -- etching of the hole through the silicon substrate and filling the hole with electroplated metal (Figure 2). Fabrication begins with the selection of an appropriate substrate. For the initial experiments, 2" n-type <100>, single-side polished, silicon wafers were chosen. The wafers were approximately 10 mils thick (250 μm) with a resistivity higher than 1 Ω-cm. An insulating layer of silicon dioxide was grown using dry thermal oxidation (Figure 2a). Thermal evaporation was then used to deposit an electroplating seed layer on the polished side of the wafer (Figure 2b). Standard photolithography techniques were used to pattern the silicon dioxide layer on the back side of the wafer. Using a potassium hydroxide solution, holes were anisotropically etched through the silicon to the seed layer from the back side of the wafer using the patterned silicon dioxide layer as an etch mask (Figure 2c). The holes were then filled with the electroplated nickel/iron alloy (Figure 2d). In the final step, the seed layer itself would be removed leaving the via filled with soft magnetic material.

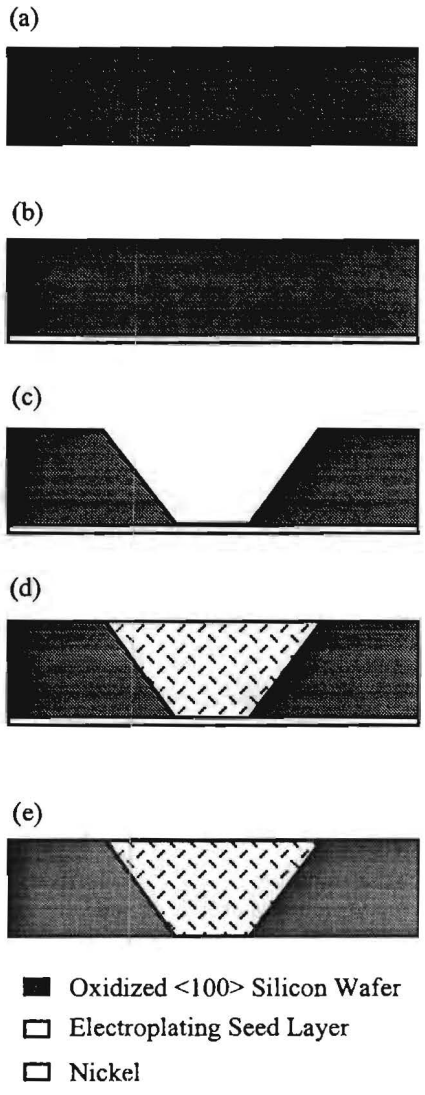

Figure 2 Test structure fabrication sequence.

2.3 Evaluation

Figure 3 shows a typical test structure fabricated using the above procedure. The dark areas of the photograph show the silicon wafer itself. The bright squares and lines are the holes that have been filled with the electroplated nickel alloy. During the fabrication of the test samples, electroplating of permalloy directly onto the silicon sidewalls of the holes was observed. When plating is initiated, the silicon is electrically isolated from the seed layer by the silicon dioxide layer. Once the hole begins to fill, however, the electroplated metal eventually touches both the seed layer and the silicon sidewalls, providing a path for current flow that results in electrodeposition onto the sidewalls. The plating of metal onto the sidewalls can potentially produce voids in the final structure that could reduce the flux capacity of the guide.

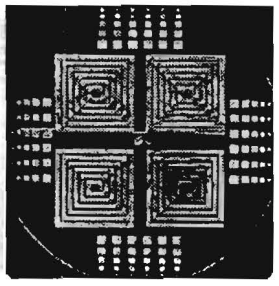

Figure 3 Photograph of a flux guide test structure fabricated using a 2", n-type silicon substrate. Small squares range in size from 20 μm to 100 μm. The 1 cm x 1 cm spiral patterns consist of lines 50 μm wide separated by 50 μm spaces.

2.4 Modifications of Fabrication Procedure

To address the sidewall plating concerns, the fabrication procedure was modified slightly. In the n-type substrate, electrons are the majority carriers. By starting with a lightly doped p-type substrate, the number of majority carriers, in this case, holes, are reduced, and the mobility of these carriers is significantly less than that of the electrons in the original samples. This should reduce the substrate's ability to conduct, and hence, the amount of sidewall plating. The p-type samples that were fabricated, however, exhibited significant plating onto the sidewalls of the holes prompting another modification of the basic procedure. To further reduce the number of carriers in the p-type samples, an optically opaque box was constructed to contain the electroplating apparatus. By shielding the sample from light during electroplating, optically generated carriers are eliminated thus reducing the substrate's ability to conduct. As before, this modification did not eliminate electroplating of metal onto the hole sidewalls.

From the above experiments it became clear that the sidewalls of the holes needed to be insulated prior to electroplating. Our first attempt at insulating the sidewalls required an additional thermal oxidation of the wafer. Starting with an oxidized silicon substrate, n-type or p-type, the front oxide layer is patterned by photolithography. Using the patterned oxide as an etch mask, a 50 μm deep trench is etched into the wafer. Note that for these experiments the hole is not etched completely through the wafer. Once the trench was etched, the sample is thermally oxidized to insulate the entire surface including the trench sidewalls. The seed layer was then deposited followed by a photoresist electroplating mold. The trench was then filled with electroplated permalloy as seen in Figure 3.

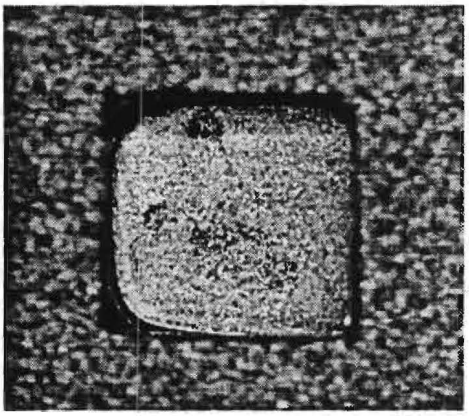

Figure 4 Photograph of nickel/iron filled trench. Side length is 800 μm.

3.0 Alternative Flux Guide Test Structure

3.1 Description

An additional test structure was made using a PC board as a substrate. A standard board was used, consisting of a 1/16" thick epoxy impregnated fiberglass board, with 3 thousandths of an inch of copper laminated on the top and bottom. As a substrate, it has the advantage of being inert and inherently electrically insulative. The test pattern used is shown below. Magnetic flux will be guided through electroplated iron nickel plugs and the horizontal surface electrodes will conduct the current. The selection of 80% nickel / 20% iron alloy (permalloy) allows for saturation flux densities on the order of 1.0 Tesla.

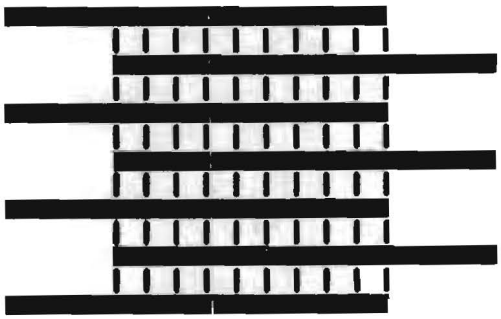

Figure 5 Mask used to pattern substrate. Length of holes, 4 mm. Width, 1 mm.

3.2 Fabrication Procedure

The first step in fabrication is to pattern the hole locations and electrodes. This was done using a direct mask derived from Figure 1 and then etching the unprotected areas using a copper etch consisting of 1/4 pound of anhydrous ferric chloride in 16 oz. of water heated to 125 F. The backside of the substrate was protected by using a commercial polystyrene film available from GC Electronics. This film is an excellent barrier to ferric chloride but is easily removed using acetone.

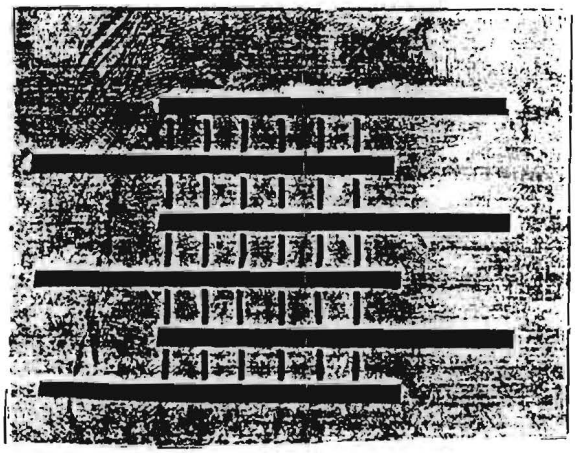

Figure 6 Image of substrate with mask lines down, prior to copper etching. (full size)

The next step is to create the holes for plating. Because of the simple geometry, orthogonal spacing and relatively large dimensions of the holes, the holes were milled out using a precision vertical mill. Etching would not be possible, since no etch exists for the substrate. However, the material can be milled to a close tolerance rapidly and without difficulty.

The next step is to plate the holes. To accomplish this, a surface must be used to plate from. In this case, the test board was backed with another copper board. Electrical contact was made at the interface using a conductive silver paint spread thinly between the surfaces. The edges and top side electrodes were sealed from the plating bath using more polystyrene film. The assembly was then placed in a 80% nickel / 20% iron plating bath and the holes were plated. Due to the thickness of the substrate (1/16"), this was the most time consuming part of the whole procedure.

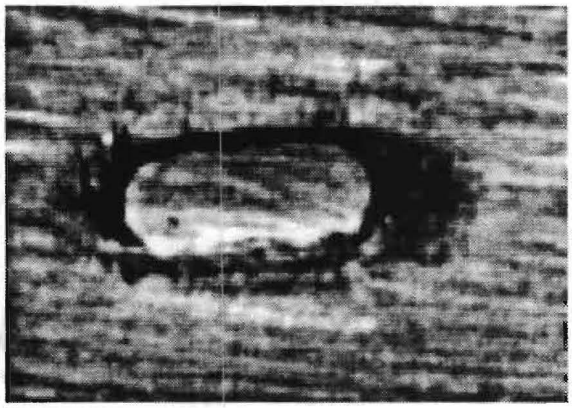

Figure 7 Image of one nickel plated hole

The last step is to release the substrate from the back plating guide by using acetone to dissolve the polystyrene and then lifting the device from the back plate. This works very well, the side wall adhesion greatly exceeds the adhesion to the lower most copper plate and the devices lift cleanly away. A final clean prepares the device for final packaging.

At this point, the device was sent to Newport, RI for integration with magnets on the back surface. The only remaining step is to isolate the top electrodes except in the desired areas. This was done off site, but involves coating the top surface and exposing the electrodes only in the required areas. I recommended a procedure and provided a sample bottle of polystyrene to accomplish this.

3.3 Conclusions

Fabricating on a PC board substrate is possible. A relatively thick board (1/16") was used in this initial test. In future trials, a thinner board would provide more flexibility and reduce processing time (since the plating height would be lower). Despite the unusual nature of this project, all steps lend themselves to batch processing and production devices could be made inexpensively in this manner.